

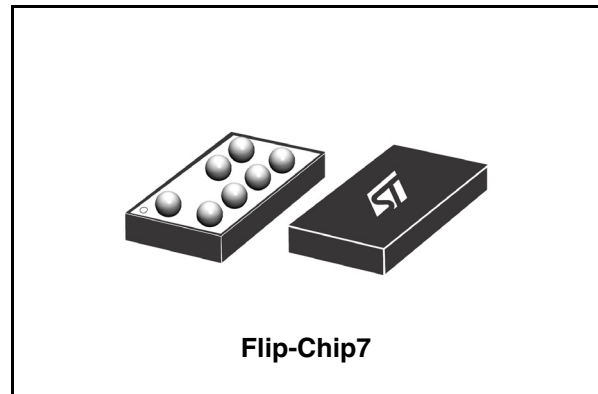


STG4159

Low voltage 0.3Ω max single SPDT switch with break-before-make feature and 10kV contact ESD protection

Features

- Wide operating voltage range:
 $V_{CC} \text{ (OPR)} = 1.65\text{V to } 4.8\text{V}$
- Low power dissipation:
 $I_{CC} = 0.2\mu\text{A (max.) at } T_A = 85^\circ\text{C}$
- Low "ON" resistance $V_{IN} = 0\text{V}$:
 - $R_{ON} = 0.40\Omega$ (max. $T_A = 25^\circ\text{C}$) at $V_{CC} = 2.25\text{V}$
 - $R_{ON} = 0.35\Omega$ (max. $T_A = 25^\circ\text{C}$) at $V_{CC} = 3.0\text{V}$
 - $R_{ON} = 0.30\Omega$ (max. $T_A = 25^\circ\text{C}$) at $V_{CC} = 4.3\text{V}$
- Separate supply voltage for switch and control pin
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD performance tested on common channel (D pin)
 - 10kV IEC-61000-4-2 ESD, contact discharge
 - 15kV IEC-61000-4-2 ESD, air discharge
- ESD performance test on all other pins
 - 10kV IEC-61000-4-2 ESD, contact discharge
 - 500V machine model (JESD22 A115-A)
 - 1500V charged-device model (JESD22 C101)



Description

The STG4159 is a high-speed CMOS low voltage single analog SPDT (Single Pole Dual Throw) switch or 2:1 multiplexer/demultiplexer switch fabricated in silicon gate C²MOS technology. It is designed to operate from 1.65V to 4.58V, making this device ideal for portable applications. It offers low ON-resistance (0.45Ω) at $V_{CC} = 4.3\text{V}$. The SEL inputs are provided to control the switches.

The switch S1 is ON (connected to common Port D) when the SEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (it is connected to common Port D) when the SEL input is held low and OFF (high impedance state exist between the two ports) when SEL is held high.

Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

Part number	Package	Packaging
STG4159	Flip-Chip7	Tube
STG4159BJR	Flip-Chip7	Tape and reel

Contents

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1 Logic diagram

Figure 1. Functional diagram

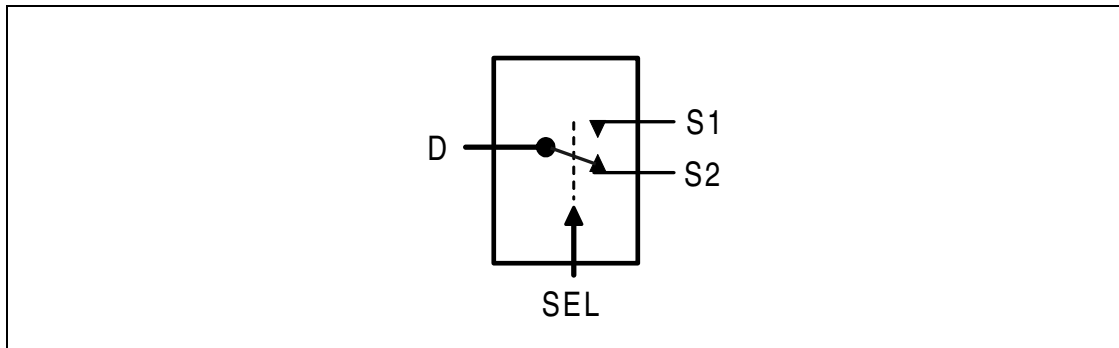


Figure 2. Input equivalent circuit

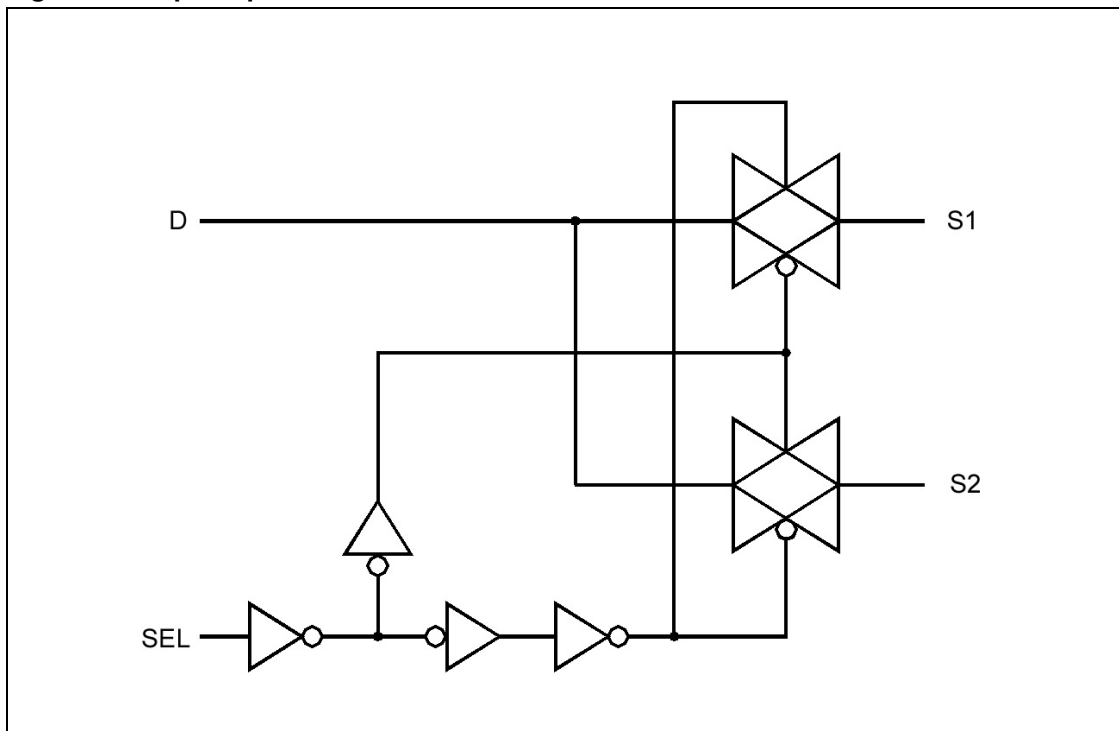


Table 2. Truth table

SEL	Switch S1	Switch S2
H	ON	OFF ⁽¹⁾
L	OFF ⁽¹⁾	ON

1. High Impedance

Figure 3. Pin connection (bump side view)

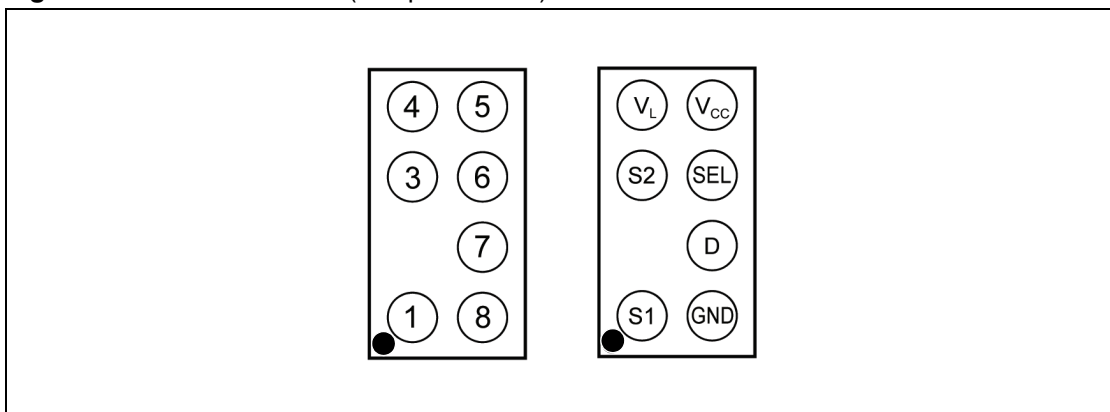


Table 3. Pin description

Flip-Chip	Symbol	Name and function
1, 3	S1, S2	Independent channels
7	D	Common channel
6	SEL	Control
5	V _{CC}	Positive supply voltage
4	V _L	Logic supply voltage
8	GND	Ground (0V)

2 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_L	Logic supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_{IC}	DC control input voltage	-0.5 to $V_L + 0.5$	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IKC}	DC input diode current on control pin ($V_{SEL} < 0V$)	-50	mA
I_{IK}	DC input diode current ($V_{SEL} < 0V$)	± 50	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 300	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	± 500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation at $T_A = 70^\circ C$ ⁽¹⁾	500	mW
T_{stg}	Storage temperature	-50 to 105	$^\circ C$
T_L	Lead temperature (10 sec)	260	$^\circ C$

1. Derate above 70 $^\circ C$ by 18.5mW/C

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	1.65 to 4.8	V
V_L	Logic supply voltage ⁽²⁾	1.65 to V_{CC}	V
V_I	Input voltage	0 to V_{CC}	V
V_{IC}	Control input voltage	0 to V_L	V
V_O	Output voltage	0 to V_{CC}	V
T_{op}	Operating temperature	-40 to 85	$^\circ C$
dt/dv	Input rise and fall time control input	$V_L = 1.65V$ to 2.7V	0 to 20
		$V_L = 3.0V$ to 4.8V	0 to 10
			ns/V

1. Truth Table guaranteed: 1.65V to 4.8V

2. V_L pin should not be left floating.

3 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test conditions			Value					Unit
		V _{CC} (V)	V _L (V)		T _A = 25°C			-40 to 85°C		
					Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High level input voltage	1.65-4.3	1.65-1.95		1.25			1.25		V
			2.3-2.7		1.75			1.75		
			3.0-3.6		2.35			2.35		
			4.3		2.8			2.8		
V _{IL}	Low level input voltage	1.65-4.3	1.65-1.95				0.6		0.6	V
			2.3-2.7				0.8		0.8	
			3.0-3.6				1.05		1.05	
			4.3				1.5		1.5	
R _{ON}	ON resistance	1.8	1.65-4.3	V _S =0V to V _{CC} I _S =100mA		0.49	0.65		0.85	Ω
		2.25				0.30	0.40		0.50	
		3				0.25	0.35		0.45	
		3.7				0.22	0.32		0.42	
		4.3				0.21	0.30		0.40	
ΔR _{ON}	ON resistance match between channels ⁽¹⁾	1.8	1.65-4.3	V _S =0V to V _{CC} I _S =100mA		5				mΩ
		2.25				3				
		3				3				
		3.7				3				
		4.3				3				
R _{FLAT}	ON resistance flatness ⁽²⁾	1.8	1.65 - 4.3	V _S =0V to V _{CC} I _S =100mA		300	400		450	mΩ
		2.5				130	170		230	
		3				90	120		170	
		3.7				90	120		170	
		4.3				90	120		170	
I _{OFF}	Sn OFF state leakage current	1.65-4.3	1.65 - 4.3	V _S =0 to V _{CC} V _D =0 to V _{CC}	-20		20	-300	300	nA
I _{ON}	Sn ON state leakage current	1.65-4.3	1.65 - 4.3	V _S =0 to V _{CC} V _D =Open	-20		20	-100	100	nA
I _D	D ON state leakage current	1.65-4.3	1.65 - 4.3	V _S =Open V _D =0 to V _{CC}	-20		20	-100	100	nA

Table 6. DC specifications

Symbol	Parameter	Test conditions			Value					Unit
		V _{CC} (V)	V _L (V)		T _A = 25°C			-40 to 85°C		
					Min.	Typ.	Max.	Min.	Max.	
I _{CC}	Quiescent supply current	1.65-4.3	1.65 - 4.3	V _{SEL} =V _{CC} or GND	-0.05		0.05	-0.2	0.2	μA
I _{SEL}	SEL leakage current	1.65-4.3	1.65 - 4.3	V _{SEL} =4.3V or GND	-0.1		0.1	-1	1	μA

1. $\Delta R_{ON} = R_{ON(Max)} - R_{ON(Min)}$

2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35pF, R_L = 50Ω, t_r = t_f ≤ 5ns)

Symbol	Parameter	Test conditions			Value					Unit
		V _{CC} (V)	V _L (V)		T _A = 25°C			-40 to 85°C		
					Min.	Typ.	Max.	Min.	Max.	
t _{PLH} , t _{PHL}	Propagation delay	1.65-1.95	1.65-4.3			0.13				ns
		2.3-2.7				0.15				
		3.0-3.3				0.16				
		3.6-4.3				0.16				
t _{ON}	TURN-ON time	1.65-1.95	1.65-4.3	V _S = V _{CC} R _L = 50Ω C _L = 30pF		95	123		160	ns
		2.3-2.7				48	62		80	
		3-3.6				33	43		56	
		4.3				29	38		49	
t _{OFF}	TURN-OFF time	1.65-1.95	1.65-4.3	V _S = V _{CC} R _L = 50Ω C _L = 30pF		12	15		20	ns
		2.3-2.7				12	16		21	
		3-3.6				13	17		22	
		4.3				13	17		22	
t _D	Break-before-make time delay	1.65-1.95	1.65-4.3	C _L = 35pF R _L = 50Ω V _S = V _{CC} /2	10	42				ns
		2.3-2.7			10	22				
		3-3.6			5	15				
		4.3			5	12				
Q	Charge injection	1.65-1.95	1.65-4.3	C _L = 1nF V _{GEN} = 0V		83				pC
		2.3-2.7				98				
		3.0-3.3				114				
		3.6-4.3				140				

Table 8. Analog switch characteristics ($C_L = 5\text{pF}$, $R_L = 50\Omega$, $T_A = 25^\circ\text{C}$)

Symbol	Parameter	Test conditions			Value					Unit	
		V_{CC} (V)	V_L (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C			
					Min.	Typ.	Max.	Min.	Max.		
OIRR	Off Isolation (1)	1.65-4.3	4.3	$V_S = 1V_{RMS}$ $f = 100\text{kHz}$		-69					dB
Xtalk	Crosstalk	1.65-4.3	4.3	$V_S = 1V_{RMS}$ $f = 100\text{kHz}$		-69					dB
THD	Total harmonic distortion	2.3-4.3	4.3	$R_L = 600\Omega$ $C_L = 50\text{pF}$ $V_S = V_{CC} V_{PP}$ $f = 600\text{Hz to } 20\text{kHz}$		0.01					%
BW	-3dB Bandwidth (switch ON)	1.65-4.3	4.3	$R_L = 50\Omega$		28					MHz
C_{SEL}	Control pin input capacitance	1.8-4.3	1.8-4.3	$V_L = V_{CC}$		30					pF
C_{Sn}	Sn port capacitance	1.8-4.3	1.8-4.3	$V_L = V_{CC}$		94					
C_D	D port capacitance when switch is enabled	1.8-4.3	1.8-4.3	$V_L = V_{CC}$		227					

1. OFF-isolation = $20 \log_{10} (V_D/V_S)$, V_D = output, V_S = input to off switch

4 Test circuits

Figure 4. ON-Resistance

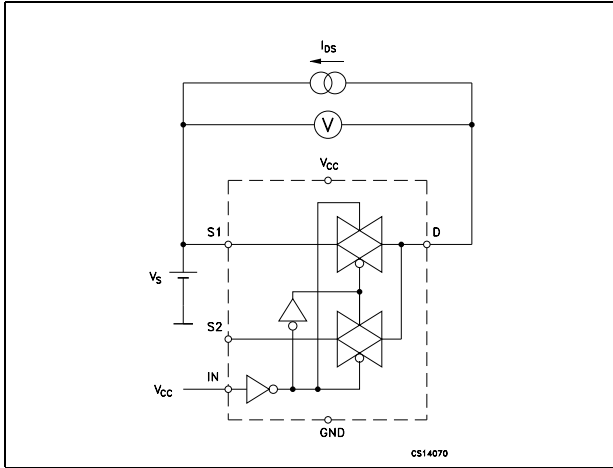


Figure 5. Bandwidth

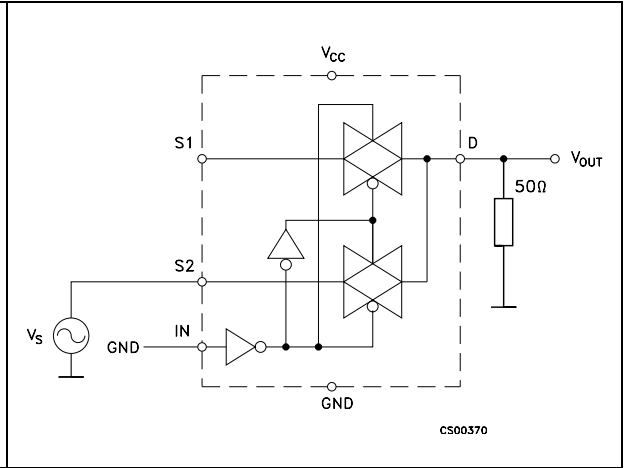


Figure 6. OFF Leakage

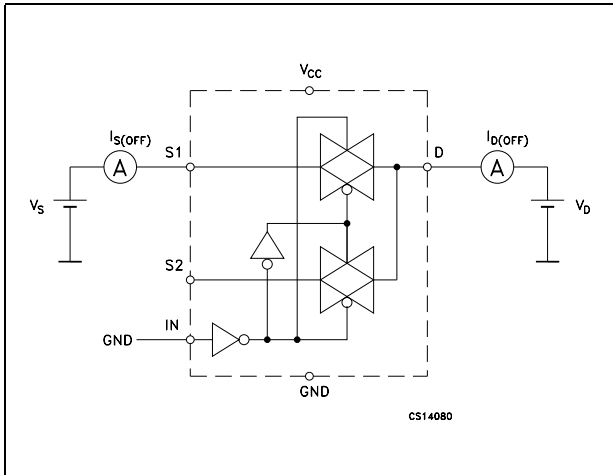


Figure 7. Channel to channel crosstalk

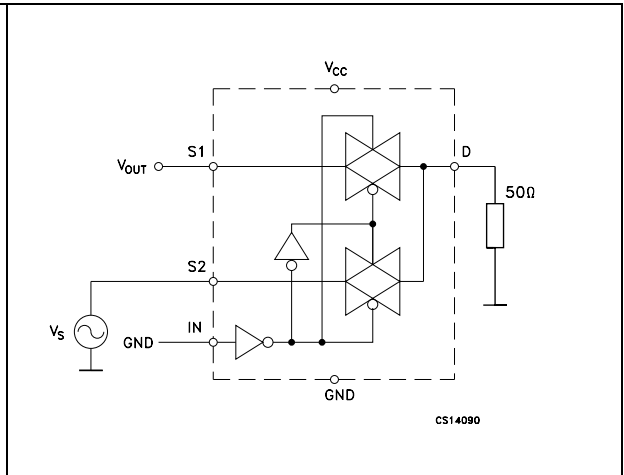


Figure 8. OFF Isolation

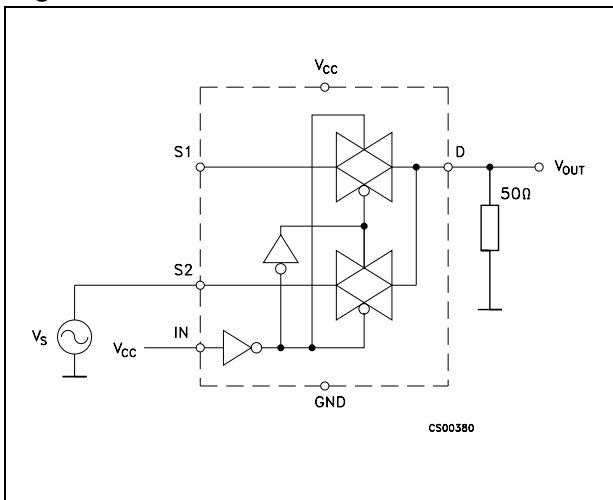
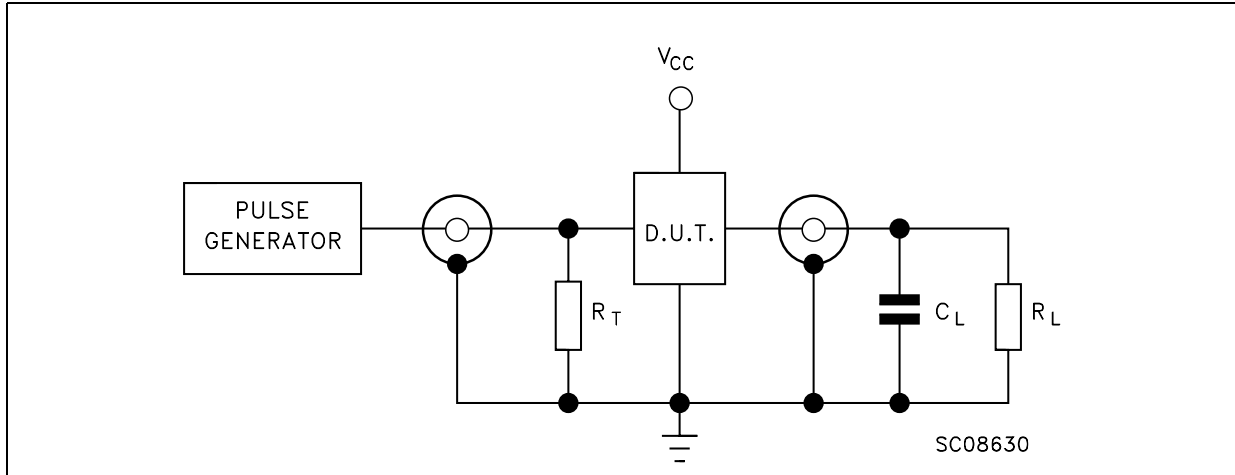


Figure 9. Test circuit



- Note: 1 $C_L = 5/35\text{pF}$ or equivalent: (includes jig capacitance)
 2 $R_L = 50\Omega$ or equivalent
 3 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 10. Break-before-make time delay

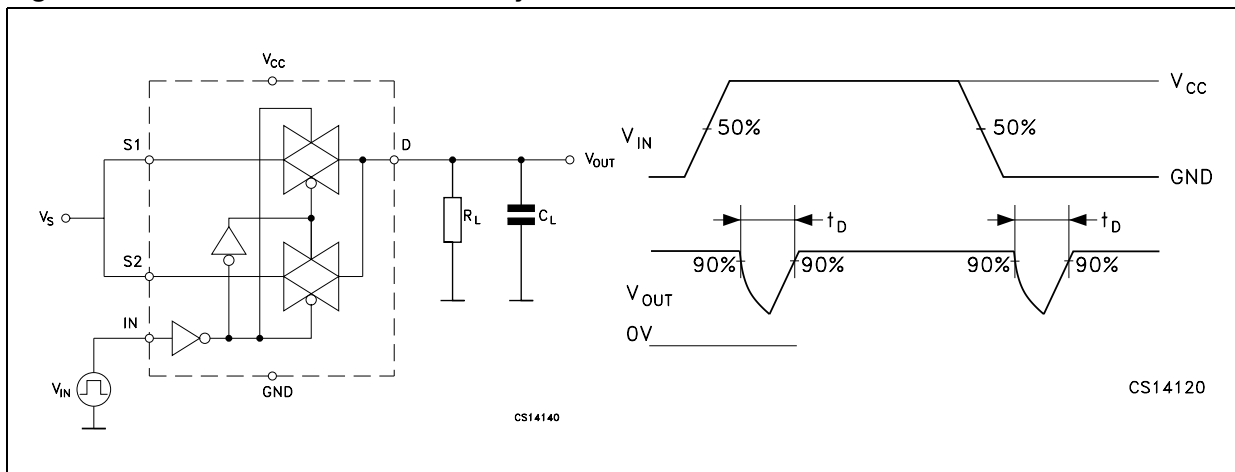


Figure 11. Switching time and charge injection
 ($V_{GEN} = 0V$, $R_{GEN} = 0\Omega$, $R_L = 1M\Omega$, $C_L = 100pF$)

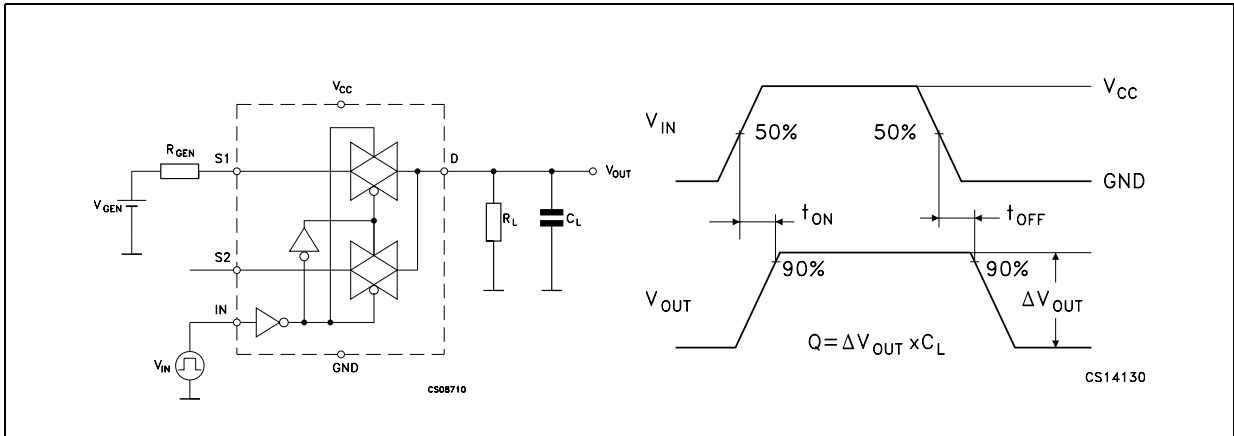
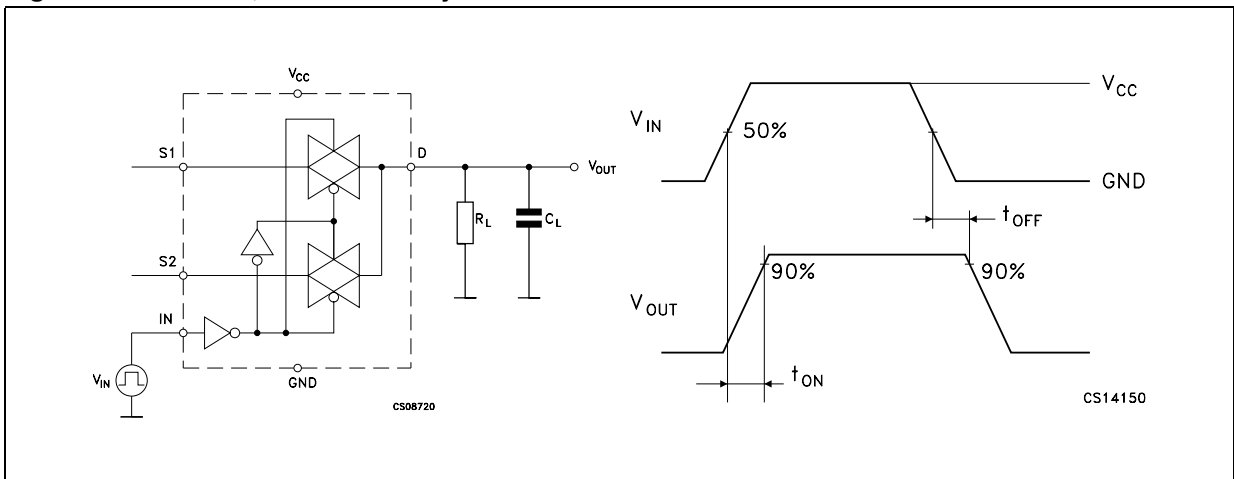


Figure 12. Turn ON, turn OFF delay time



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 9. Flip-Chip7 mechanical data

Dim.	Data book (mm)			Drawing (mm)		
	Min	Typ	Max	Min	Typ	Max
A	0.585	0.65	0.715	0.60	0.65	0.70
A1	0.21	0.25	0.29	0.22	0.25	0.28
A2		0.4		0.38	0.4	0.42
b	0.265	0.315	0.365	0.290	0.315	0.340
D	1.018	1.068	1.118	1.053	1.068	1.083
D1		0.5		0.49	0.5	0.51
E	2.018	2.068	2.118	2.053	2.068	2.083
E1		1.5		1.49	1.5	1.51
e	0.45	0.5	0.55	0.46	0.5	0.54
f		0.284		0.272	0.284	0.292
ccc		0.08			0.08	

Note: 1 The terminal Pin 1 on the bumps side is identified by a distinguishing feature (for instance by a circular "clear area" - typically 0.1mm diameter -) The terminal Pin 1 on the backside of the product is identified by a distinguishing feature (for instance by a circular "dot" - typically 0.5mm diameter -).

Figure 13. Package dimensions

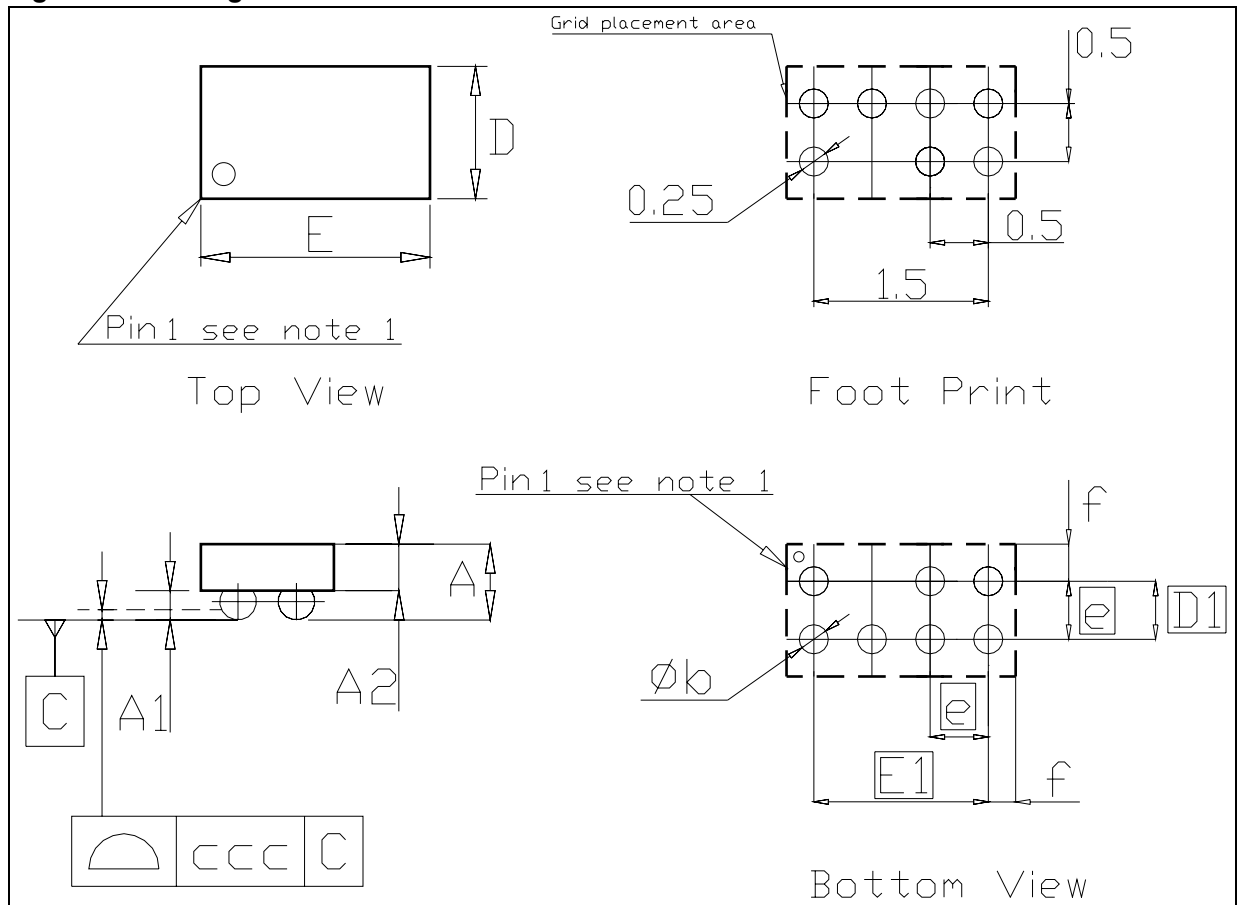


Figure 14. Foot print recommendations

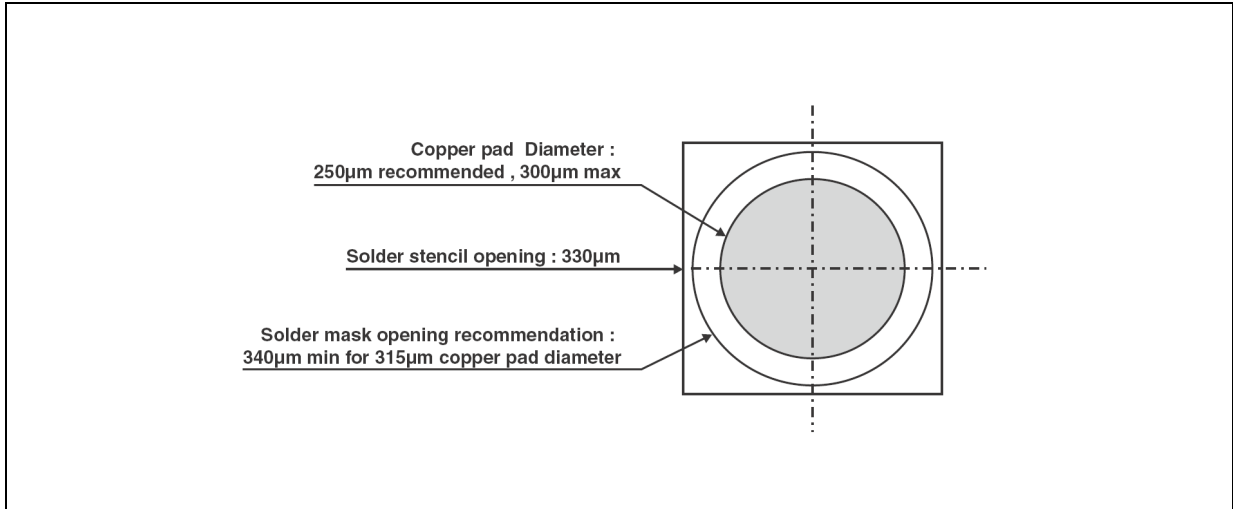


Figure 15. Marking

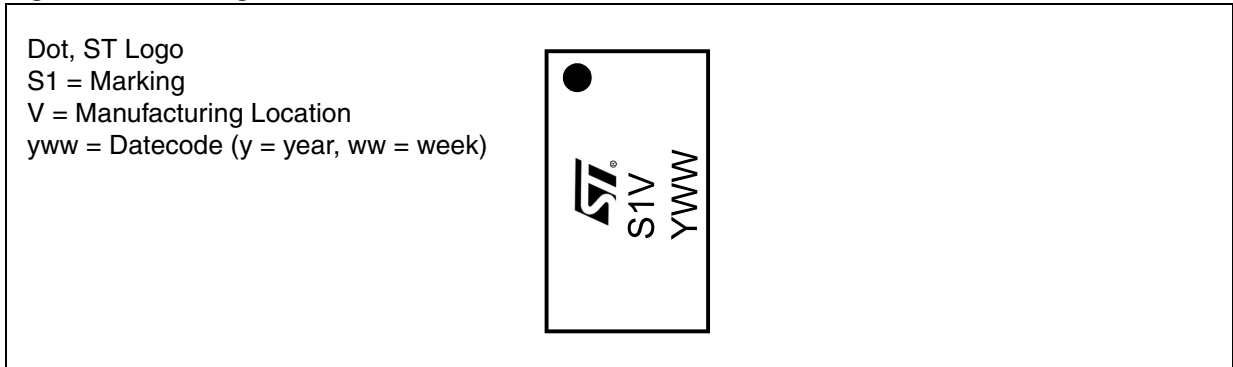


Figure 16. Flip-Chip7 tape specification

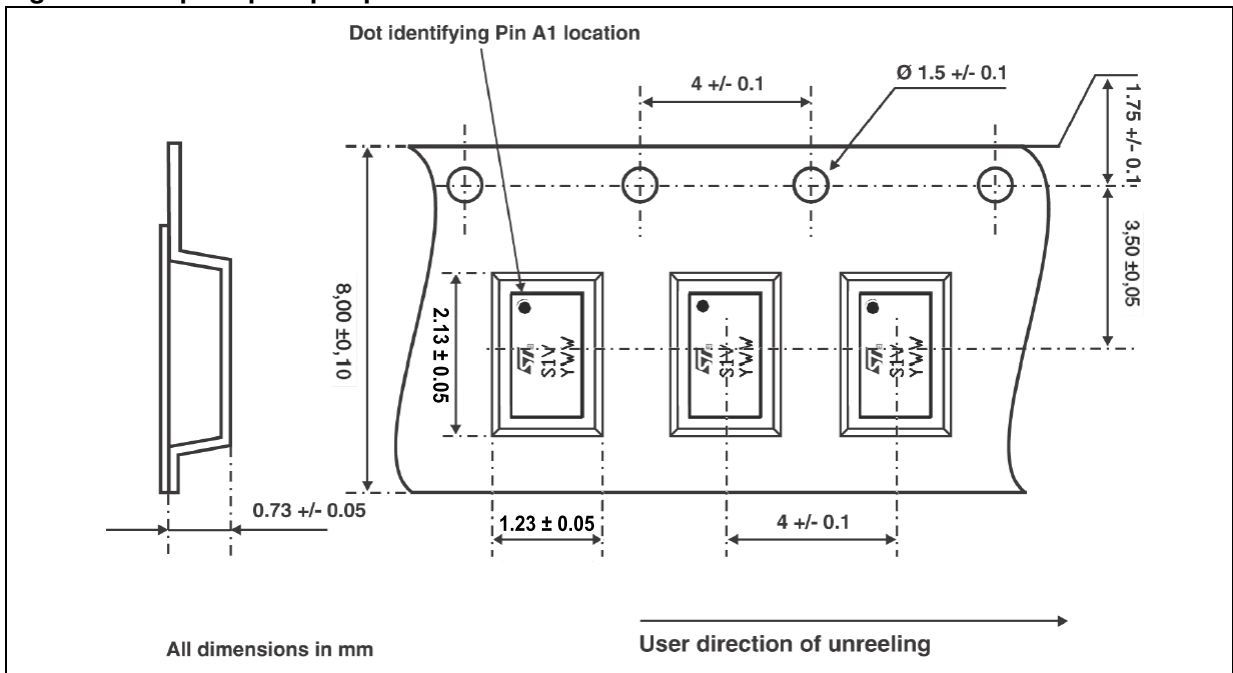


Figure 17. Flip-Chip7 reel information

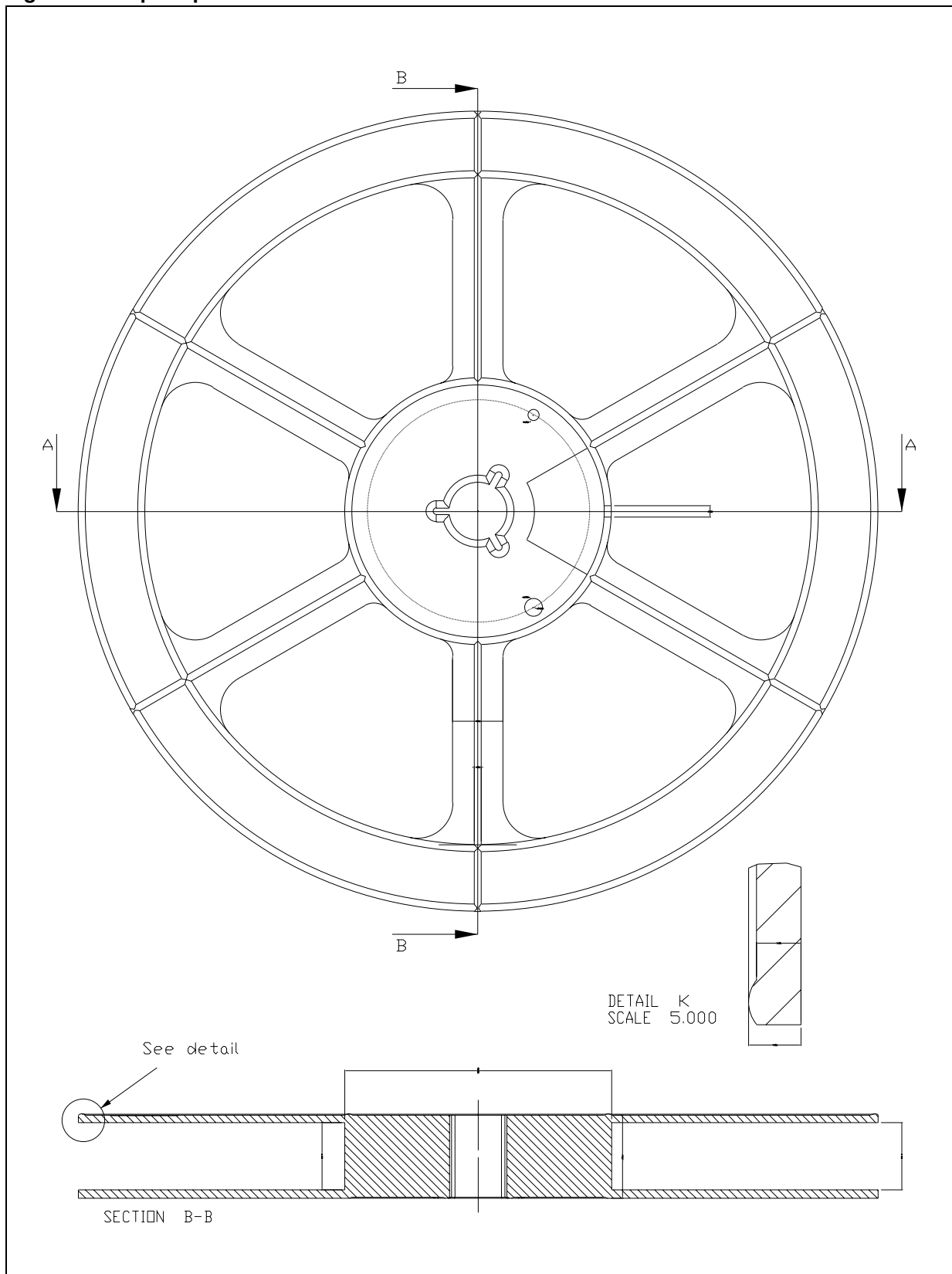
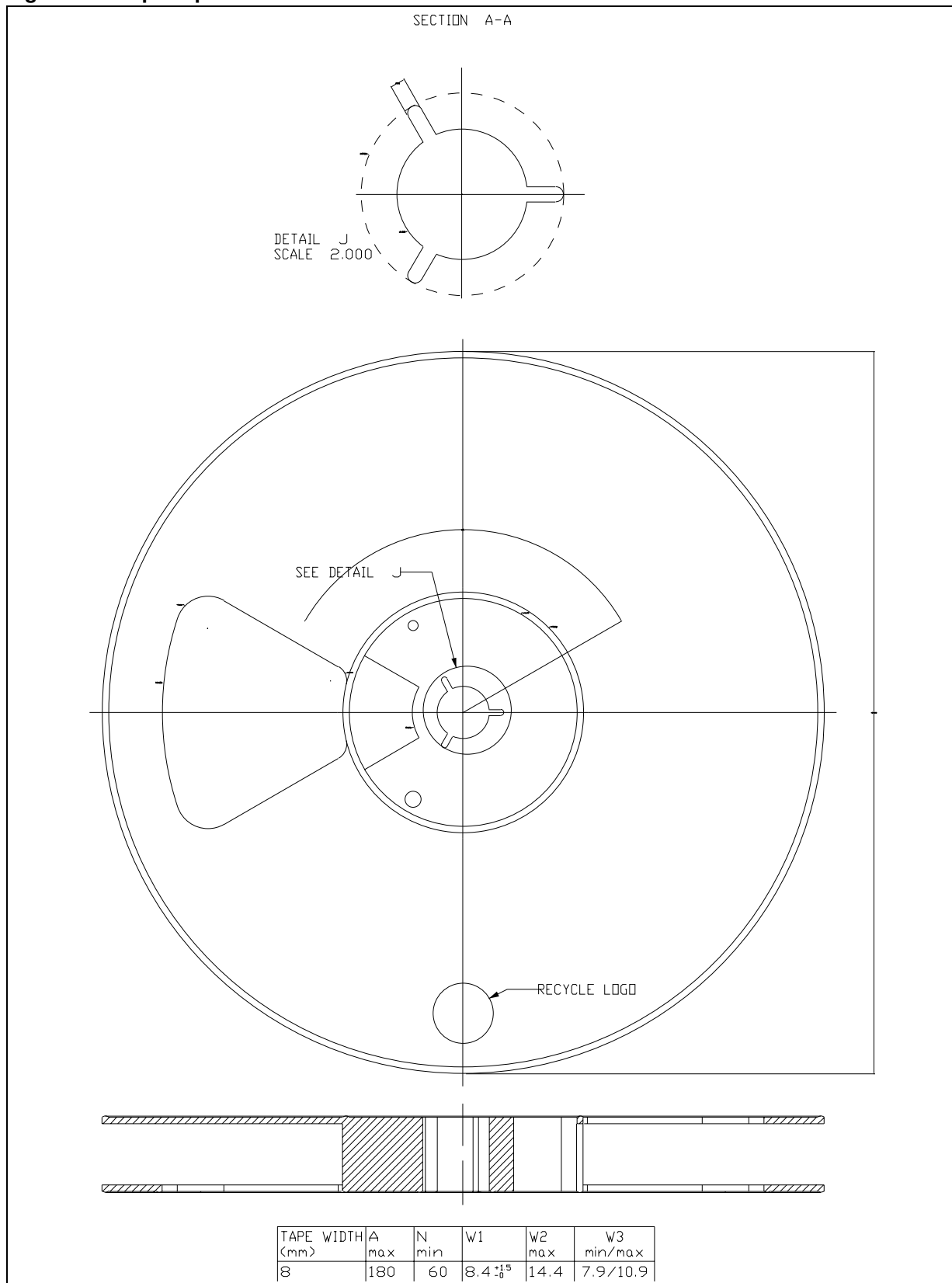


Figure 18. Flip-Chip7 reel information



6 Revision history

Table 10. Revision history

Date	Revision	Changes
05-May-2006	1	First release
22-Nov-2006	2	Schematic <i>Figure 1 on page 3</i> updated
17-Apr-2007	3	Typo in cover page description

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